ABSTRACT OF THE DISCLOSURE

Disclosed is a multiprocessor system in which even if contention occurs when a common memory is accessed from each of a plurality of processors, the number of times the common memory is accessed is capable of being reduced. The common memory of the multiprocessor system is provided with a number of data areas that store data and with a control information area that stores control information indicating whether each of the data areas is in use, and each processor is provided with a storage unit equivalent to the common memory and with an access controller. The access controller of a processor that does not have access privilege monitors data and addresses that flow on the common bus, accepts data written to the common memory and data read from the common memory, and stores this data in the storage unit of its own processor, thereby storing content identical with that of the common memory.